CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. (Previously Presented) A circuit arrangement for rapidly switching an inductive load, said arrangement comprising:

- a switching transistor implemented as an N-channel MOS power transistor and connected as a high-side switch for connecting a load with a supply voltage,

- controllable switching means for applying a potential exceeding the voltage of the supply voltage source to a gate electrode of the switching transistor, said switching means incorporating at least a first switching-means transistor whose collector current flows at least in part to the gate electrode of the switching transistor during the ON state, said first switching-means transistor is connected as a current source, said first switching-means transistor is part of a current mirror circuit, wherein the current mirror circuit incorporates a first current mirror resistor and a second current mirror resistor each connected to a low voltage source, the first current mirror resistor being connected to the base electrode and the second current mirror resistor being connected to the emitter electrode of the first switching-means transistor.

2. (Cancelled)

3. (Cancelled)

4. (Previously Presented) A circuit arrangement according to Claim 1, wherein the first switching-means transistor is a pnp transistor.

5. (Previously Presented) A circuit arrangement according to Claim 1, wherein the collector current of the first switching-means transistor flows to the gate electrode of the switching transistor via a diode connected in the flow direction.

6. (Previously Presented) A circuit arrangement according to Claim 1, wherein the ratio of the resistance values of the first current mirror resistor and the second current mirror resistor corresponds to approximately 100:1.

7. (Previously Presented) A circuit arrangement according to Claim 1, wherein an input current of the current mirror circuit is controllable by means of a second switching-means transistor connected as a current source and clocked by a control signal.

8. (Previously Presented) A circuit arrangement according to Claim 7, wherein the input current of the current mirror flows to the latter via an RC element comprising an RC element resistor and a parallel-connected RC element capacitor.

9. (Previously Presented) A circuit arrangement according to Claim 8, wherein the time constant of the RC element is so designed that the RC element-capacitor is not charged significantly during the turn-on time of the switching transistor, but virtually completely charged during its ON time.

10. (Previously Presented) A circuit arrangement according to Claim 1, wherein the current mirror circuit further includes a diode connected in series with the first current mirror resistor and in the flow direction of the current mirror input current.

11. (Previously Presented) A circuit arrangement according to Claim 1, wherein a bootstrap capacitor is provided which is connected to the low voltage source and to the source electrode of the switching transistor.

12. (Previously Presented) A circuit arrangement according to Claim 1, wherein there is provided a bootstrap diode oriented in the forward direction for coupling the voltage of the low voltage source into the current mirror circuit.

13. (Previously Presented) A circuit arrangement according to Claim 1, wherein the low voltage source has an auxiliary voltage source sitting on top of the potential of the supply voltage.

14. (Previously Presented) A circuit arrangement according to Claim 1, further comprising a second switching-means transistor whose emitter electrode is connected to the gate electrode of the switching transistor and whose collector electrode is connected via a leakage resistor to the source electrode of the switching transistor.

15. (Previously Presented) A circuit arrangement according to Claim 14, further comprising a third switching means transistor wherein the base electrode of the third switching-means transistor is connected via a leakage resistor to the source electrode of the switching transistor.

16. (Previously Presented) A circuit arrangement according to Claim 14, wherein the second switching-means transistor is a pnp transistor.

17. (Previously Presented) A circuit arrangement according to Claim 5, further comprising a second switching-means transistor whose emitter electrode is connected to the gate electrode of the switching transistor and whose collector electrode is connected via a leakage resistor to the source electrode of the switching transistor.

18 - 22. (Cancelled)